

## LIST OF REFERENCES CITED BY APPLICANT

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ATTY. DOCKET NO.

9797-050-999

APPLICATION NO.

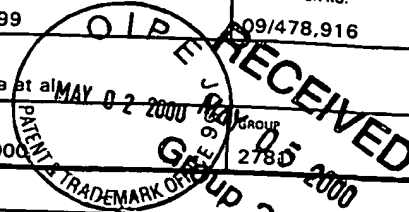
09/478,916

APPLICANT

Jared L. Zerbe et al.

FILING DATE

January 6, 2000



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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
W	AA	5,194,765	Mar. 16, 1993	Dunlop et al.	307	443	Jun 28, 1991
	AB	5,254,883	Oct. 19, 1993	Horowitz et al.	307	443	Apr 22, 1992
	AC	5,513,327	Apr. 30, 1996	Farmwald et al.	395	309	Mar 31, 1994
	AD	5,023,488	Jun. 11, 1991	Gunning	307	475	Mar 30, 1990
	AE	5,483,110	Jan. 9, 1996	Koide et al.	307	147	Feb 28, 1994
	AF	5,287,108	Feb. 15, 1994	Mayes et al.	341	156	Jul 2, 1992
W	AG	5,977,798	Nov. 2, 1999	Zerbe	326	98	Jul 18, 1997

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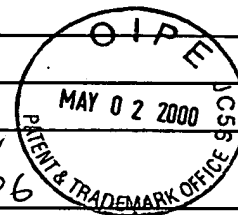
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
W	AH	EP 0 463 316 A1	02 Jan 92	DE FR GB	H04L	12/40	X
W	AI	EP 0 482 392 A2	29 Apr 92	AT BE CH DE DK ES FR GB IT LI NL SE	H04L	25/08	X
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	AM	Allen, Arnold O.; "Probability, Statistics, and Queueing Theory with Computer Science Applications"; 2 <sup>nd</sup> Edition, CH 7; pp. 450, 458-459.
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							YES	NO
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we	AQ	Taborek; "Multi-Level Analog Signaling Techniques for 10 Gigabit Ethernet"; IEEE 802.3 Tutorial.
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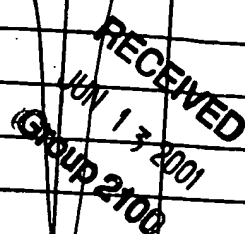
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		6,140,841	10/31/00	Suh				
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							YES	NO
<i>we</i>	EO	DE 43 20 930	01/05/95	Germany (Kommunikations Elektronik)				
	EP	EP 0 094 624	11/23/83	EPO (Siemens AG)				
	EQ	EP 0 490 504 A2	06/07/92	EPO (Northern Telecom Limited)				
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	FB	JP 08286943	11/01/96	Japan (Takaoka Electric Mfg Co Ltd)				
	FC	JP 09181778	07/11/97	Japan (Aiphone Co Ltd)				
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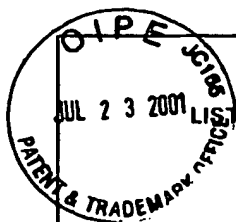
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						YES	NO
we	JP60191231	8/30/85	Japan	X	X	X	
we	JP56168711	10/23/81	Japan			X	
we	JP52127887	10/24/77	Japan			X	

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PTO-1449				Application Number	09/478,916
				Filing Date	January 6, 2000
				First Named Inventor	Jared L. Zerbe et al.
				Art Unit	2189
				Examiner Name	Tim T. Vo
				Attorney Docket Number	9797-0050-999

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
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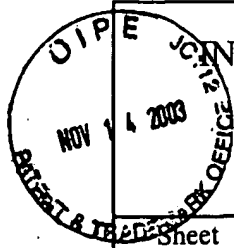
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Art Unit	2189
Examiner Name	Tim T. Vo
Attorney Docket Number	9797-0050-999

Sheet

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of

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<i>we</i>	5,757,712	5/26/98	Nagel et al.			
	5,798,918	8/25/98	Georgiou et al.			
	5,809,033	9/15/98	Turner et al.			
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	6,215,635	4/10/01	Nguyen			
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<i>we</i>	6,262,611	7/17/01	Takeuchi			

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Examiner  
Signature*Tim T. Vo*Date  
Considered

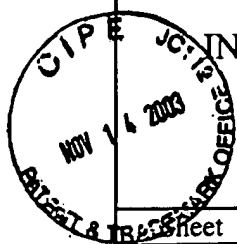
11/5/06

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INFORMATION DISCLOSURE  
CITATION

PTO-1449

Complete If Known

Application Number	09/478,916
Filing Date	January 6, 2000
First Named Inventor	Jared L. Zerbe et al.
Art Unit	2189
Examiner Name	Tim T. Vo
Attorney Docket Number	9797-0050-999

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<i>we</i>	6,275,540	8/14/01	Barrett, Jr., et al.	<div>RECEIVED NOV 20 2003 Technology Center 2100</div>
	6,282,184	8/28/01	Lehman et al.	
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<i>we</i>	6,397,408	6/4/02	Veloskey et al.	

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
YES	NO						
<i>we</i>		JP10200345	7/31/98	Japan			X
<i>we</i>		WO 98/33306	7/30/98	WIPO			X
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<i>we</i>	Ariyavisitakul, S., "Reduced-Complexity Equalization Techniques for broadband wireless Channels," (1997), <i>IEEE Journal on Selected Areas in Communications</i> , 15(1), pp. 5-15.
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Examiner Signature	<i>Lin Sh</i>	Date Considered	11/5/06
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	Perez-Alvarez, I.A., et al., "A Differential Error Reference Adaptive Echo Canceller for Multilevel PAM Line Codes," (1996), <i>IEEE</i> , pp. 1707-1710.
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	"Propagation Over Multiple Parallel Transmission Lines Via Modes," IBM Technical Disclosure Bulletin, (April 1990). pp. 1-6.
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	IEEE - 802.3ab - A Tutorial Presentation, March 1998.
<i>we</i>	IEEE - P802.3ad-Draft Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method & Physical Layer Specifications: Link Aggregation," (1999).

Examiner Signature	<i>Tim Vo</i>	Date Considered	1/5/06
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